REMARKS/ARGUMENTS

Claims 1 - 6, and 15 are pending. Claim 15 has been amended

Claim 1 was rejected under 35 U.S.C. § 102(b) for allegedly being anticipated by Chi et al., U.S. Patent No. 5,587.596. Claim 2 was rejected under 35 U.S.C. § 103(a) for allegedly being unpatentable over Chi et al. in view of Muro, U.S. Patent No. 4,877,951.

It is noted with appreciation that claim 6 is allowable. It is further noted that dependent claims 3 - 5 are deemed to recite allowable subject matter. However, for at least the reasons set forth below, it is earnestly believed that independent claim 1 as originally filed is patentable over the cited art. Therefore, counsel for Applicant respectfully requests reconsideration of the claims in view of the remarks which follow.

It appears claim 15 was inadvertently overlooked and thus not examined. The application as originally filed included claims 1 - 15. A preliminary amendment filed with the instant application canceled claims 7 - 14, leaving claims 1 - 6 and 15 for examination. Claim 15 as amended is believed to be patentable over the cited art. Consideration of claim 15 is respectfully requested.

(i) Present Invention

The present invention relates to an image sensor. An aspect of the invention as recited in claim 1, for example, is "a peripheral circuit formed on a first region of the semiconductor substrate" where the first region is at ground voltage. A further aspect of the invention is "a plurality of unit pixels formed on a second region of the semiconductor substrate, wherein the first region is isolated from the second region" and "a negative voltage level is applied to the second region."

(ii) Cited Art

Chi et al. show a pixel transistor 114 formed in a p-well 112, which in turn, is formed in a substrate 110. The pixel transistor 114 includes source and drain regions 116 and 118, respectively. The pixel transistor further includes a channel region 120, over which a dielectric material 122 is deposited and a conductive gate 124. A p-well 130 is formed,

separated from the p-well 112. A parasitic transistor is formed between the p-wells 130 and 112 by the gate structure comprising dielectric 134 and gate layer 136.

(iii) Distinctions Between Present Invention and Cited Art

The Office action asserts that Chi et al. show "unit pixels 114 formed on a second region of the semiconductor substrate." O.A. at page 2. The Office action further asserts that "a negative voltage level is applied to the second region; it is inherent that the -5V potential (Vbb) is provided by a certain voltage circuit." *Id.* It is believed, therefore, that the Office action asserts the p-well region 112 corresponds to the recited "second region", since the unit pixel (identified as transistor 114) is formed in the p-well region 112 and Vbb is applied to the p-well region 112.

The Office action also asserts that Chi et al. show "a peripheral circuit formed on a first region ... wherein a ground voltage level (GND source 116) is applied to the first region." *Id.* Respectfully, however, there appears to be no structure in Chi et al. that corresponds to the recited "first region" and the recited "peripheral circuit formed on a first region." First, it is earnestly submitted that the p-well region 112 cannot be the recited "first region" because the p-well region was asserted as being the recited "second region." Assuming *arguendo* that assertion to be correct, then the p-well region cannot both the first region and the second region, especially since an aspect of the claim is "the first region is isolated from the second region."

Second, it is earnestly submitted further that the region 116 cannot be the recited "first region" because the region 116 has no "peripheral circuit formed on a first region." Chi et al. disclose region 116 to be a source region. It comprises an amount of n^+-doped material and there is no peripheral circuit formed on it.

For at least either of the foregoing reasons, Chi et al. do not show the recited "peripheral circuit formed on a first region of the semiconductor substrate, wherein a ground voltage level is applied to the first region." The Section 102 rejection is believed to be overcome.

(iv) Claim 15 is Patentably Distinct from the Cited Art

The invention as recited in claim 15 includes "providing a ground reference in a first region" and "providing a bias generator in the first region." Claim 15 further recites "providing a photodiode device in a second region ... including spacing apart the first region and the second region and isolating the second region from the first region."

Chi et al. do not show these aspects of the invention. Chi et al. show the source region 116 is connected to Vss. Such structure does not constitute "providing a ground reference in a first region" and "providing a bias generator in the first region." The source region 116 has no circuitry formed on it.

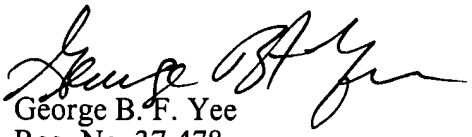
Chi et al. show pixel transistor 114 is formed in p-well 112. Since Chi et al. do not show a first region as recited in claim 15, it follows that Chi et al. do not show or suggest "spacing apart the first region and the second region" or "isolating the second region from the first region."

CONCLUSION

In view of the foregoing, all claims now pending in this Application are believed to be in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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